JPEG XS Encoder/Decoder(FPGA)

Powered by original computing algorithm “DMNA” based on mathematical methods

1 Abstract

TMC's JPEG XS encoder/decoder IP is a visually lossless compression/decompression hardware RTL core that complies with ISO/IEC-21122-1 (JPEG XS).

It is very compact, fast, and optimized for FPGAs.

2 Features

- Next-generation mezzanine compression for large screens and ultra-low latency -

- No external memory required, eliminating complex timing and bandwidth design
- Streamlined interface for fast development
- Advanced Processing: 4K/60p capability on Kintex UltraScale+ or Arria10 FPGAs
- Proven Technology: Built on our established expertise in codec development
- Two types of IPs are available for different purposes
  - Standard / Performance-oriented

3 Specification

JPEG XS DMNA

- Compression format
  - JPEG XS (ISO/IEC21122-1)
    Supported profiles: Light422.10 , Light444.12 , Main422.10 , Main444.12 , High444.12
- Compression and decompression throughput
  - 8sample/clock(Standard version) / 12sample/clock(Performance-oriented version)
- Image size (width x height) and frame rate
  - 32 x 4 pixels to 4096 x 2160 pixels (changeable on request), 60fps
- Image formats and bit depth
  - format : RGB, YCbCr4:4:4/4:2:2/4:0:0 , bit depth : 8/10/12 bit
- Image data, compressed data interface
  - image data : AXI4-Stream , 96 or 144 bit/clock
  - compressed data : AXI4-Stream , 128 bit/clock

4 Contents of Two Types

- Standard
  Operating frequency : 150MHz(YCbCr4:2:2,YCbCr4:0:0), 240MHz(RGB,YCbCr4:4:4)
- Performance-oriented
  Operating frequency : 150MHz (all formats/bit depth)
  while other companies’ IPs require 240MHz(RGB,YCbCr4:4:4)

Note Specifications are subject to change without notice

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